

## CLAIMS

What is claimed is:

- 1    1.    A method for performing a delayed transaction, comprising:  
2            receiving a read request from a PCI (Peripheral Component Interconnect)  
3    agent coupled to a PCI bridge;  
4            allocating a pre-fetch buffer for the delayed transaction;  
5            setting a buffer fill watermark for the pre-fetch buffer;  
6            transferring data into the pre-fetch buffer while monitoring a fill level of the  
7    pre-fetch buffer; and  
8            enabling data to be transferred from the pre-fetch buffer to the PCI agent  
9    once the fill level of the pre-fetch buffer meets or exceeds the buffer fill watermark.
- 1    2.    The method of claim 1, further comprising programming a configuration  
2    register on the PCI bridge to set the buffer fill watermark.
- 1    3.    The method of claim 1, further comprising determining a buffer fill watermark  
2    value by observing data transfer rates of the PCI agent when different watermarks  
3    are used.
- 1    4.    The method of claim 3, further comprising dynamically setting the buffer fill  
2    watermark value.
- 1    5.    The method of claim 1, further comprising:

2 (a) receiving a first read request to transfer data from system memory to  
3 the PCI agent, the first read request referencing an initial starting address at which  
4 the data is located;

5 (b) setting the buffer fill watermark to an initial value;

6 (c) receiving a current portion of the data at the PCI bridge;

7 (d) transferring at least part of the current portion of the data into the pre-  
8 fetch buffer while monitoring a fill level of the pre-fetch buffer;

9 (e) connecting the PCI agent to the PCI bridge in response to determining  
10 the fill level of the pre-fetch buffer meets or exceeds the buffer fill watermark;

11 (f) transferring data from the pre-fetch buffer to the PCI agent until the  
12 pre-fetch buffer is emptied or the PCI agent disconnects;

13 (g) receiving one or more subsequent read requests from the PCI agent,  
14 each subsequent read request having a starting address corresponding to a  
15 remaining portion of the data that has yet to be received by the PCI agent;

16 (h) repeating operations (c) – (g) until the data transaction is completed.

1 6. The method of claim 5, wherein the PCI agent comprises a multi-channel PCI  
2 device, and a respective set of operations (a)-(j) is performed for each channel to  
3 perform a plurality of concurrent delayed transactions.

1 7. The method of claim 6, wherein the multi-channel PCI device comprises a  
2 dual-channel mass storage device controller.

1 8. A method comprising:

2 receiving first and second data transfer requests from a multi-channel PCI  
3 (Peripheral Component Interconnect) device, the first data transfer request

4 corresponding to a first channel, the second data transfer request corresponding to a  
5 second channel;

6 initiating respective first and second delayed transactions corresponding to  
7 the first and second data transfer requests at a PCI bridge;

8 setting up a first pre-fetch buffer corresponding to the first delayed  
9 transaction, the first pre-fetch buffer having a first buffer fill watermark;

10 setting up a second pre-fetch buffer corresponding to the second delayed  
11 transaction, the second pre-fetch buffer having a second buffer fill watermark;

12 monitoring each of the first and second pre-fetch buffers to determine if the fill  
13 lever of a buffer meets or exceeds its buffer fill watermark, that pre-fetch buffer being  
14 a first filled buffer;

15 and in response thereto,

16 connecting the multi-channel PCI device to the PCI bridge;

17 mapping a virtual buffer to the first filled buffer;

18 transferring data from the first filled buffer to multi-channel PCI device until  
19 the first filled buffer is empty; and

20 disconnecting the multi-channel PCI device from the PCI bridge.

1 9. The method of claim 8, further comprising:

2 determining that a pre-fetch buffer other than the first filled buffer has been  
3 filled to meet or exceed its buffer fill watermark, said pre-fetch buffer being a second  
4 filled buffer;

5 and in response thereto,

6 connecting the multi-channel PCI device to the PCI bridge; and

7 mapping the virtual buffer to the second filled buffer;

8 transferring data from the second filled buffer to the multi-channel PCI device  
9 until the second filled buffer is empty; and

10            disconnecting the multi-channel PCI device from the PCI bridge.

1    10.    The method of claim 8, wherein the multi-channel PCI device comprises a  
2    mass storage controller.

1    11.    The method of claim 10, wherein the multi-channel PCI device comprises a  
2    dual-channel PCI SCSI (Small Computer System Interface) controller.

1    12.    The method of claim 8, wherein each of the first and second data transfers  
2    comprises a transfer of data stored in memory to the multi-channel PCI device.

1    13.    The method of claim 8, wherein the PCI bridge comprises a host-to-PCI  
2    bridge.

1    14.    The method of claim 8, wherein the PCI bridge comprises a PCI-to-PCI  
2    bridge.

1    15.    An apparatus, comprising:  
2           an integrated circuit comprising circuitry to effectuate a PCI (Peripheral  
3    Component Interconnect) bridge, including:  
4           a primary bus unit including a primary bus interface;  
5           a secondary bus unit including a secondary bus interface; and  
6           programmed logic to perform operations including:  
7           receiving first and second read requests from a multi-channel  
8           PCI device coupled to the secondary bus interface, the first read  
9           request corresponding to a first channel and having an initial size, the

10 second read request corresponding to a second channel and having  
11 an initial size;  
12 initiating respective first and second delayed transactions  
13 corresponding to the first and second read requests;  
14 setting up a first pre-fetch buffer corresponding to the first  
15 delayed transaction, the first pre-fetch buffer having a first buffer fill  
16 watermark;  
17 setting up a second pre-fetch buffer corresponding to the  
18 second delayed transaction, the second pre-fetch buffer having a  
19 second buffer fill watermark;  
20 monitoring each of the first and second pre-fetch buffers to  
21 determine if the fill level of a buffer meets or exceeds its buffer fill  
22 watermark, that pre-fetch buffer being a first filled buffer;  
23 and in response thereto,  
24 connecting the multi-channel PCI device to the secondary bus  
25 unit; and  
26 mapping a virtual buffer to the first filled buffer;  
27 transferring data from the first filled buffer to the multi-channel  
28 PCI device until the first filled buffer is empty; and  
29 disconnecting the multi-channel PCI device from the secondary  
30 bus unit.

1 16. The apparatus of claim 15, further comprising programmed logic to perform  
2 operations including:  
3 determining that a pre-fetch buffer other than the first filled buffer has been  
4 filled to meet or exceed its buffer fill watermark, said pre-fetch buffer being a second  
5 filled buffer;

6           and in response thereto,  
7           connecting the multi-channel PCI device to the secondary bus unit;  
8           mapping the virtual buffer to the second filled buffer;  
9           transferring data from the second filled buffer to the multi-channel PCI device  
10          until the second filled buffer is empty; and  
11          disconnecting the multi-channel PCI device from the secondary bus unit.

1    17.    The apparatus of claim 15, further comprising programmed logic to perform  
2    operations including:

3           receiving a subsequent read request corresponding to the first read request;  
4           determining whether a size of the subsequent read request is less than the  
5    first buffer fill watermark; and  
6           in response thereto,  
7           setting the second buffer fill watermark equal to the size of the subsequent  
8    read request.

1    18.    The apparatus of claim 17, further comprising:  
2           a plurality of configuration registers, each including a field to define a size of a  
3    subsequent read request buffer fill watermark

1    19.    The apparatus of claim 15, wherein the primary bus interface comprises an  
2    interface to a host bus and the secondary bus interface comprises an interface to a  
3    PCI root bus.

1    20.    The apparatus of claim 15, wherein each of the first and secondary bus  
2    interfaces comprises an interface to a PCI bus.

1 21. The apparatus of claim 15, further comprising a configuration register to store  
2 a buffer fill watermark value.

1 22. A computing platform, comprising:  
2 a motherboard including a host bus and a PCI (Peripheral Component  
3 Interconnect) bus;  
4 a processor operatively coupled to the host bus;  
5 memory operatively coupled to the host bus; and  
6 a host-to-PCI bridge including a primary bus unit having an interface coupled  
7 to the host bus and a secondary bus unit having an interface coupled to the PCI bus,  
8 the host-to-PCI bridge further including programmed logic to perform operations  
9 including:

10 receiving first and second read requests from a multi-channel PCI  
11 device coupled to the PCI bus, the first read request corresponding to a first  
12 channel and having an initial size, the second read request corresponding to  
13 a second channel and having an initial size;

14 initiating respective first and second delayed transactions  
15 corresponding to the first and second read requests;

16 setting up a first pre-fetch buffer corresponding to the first delayed  
17 transaction, the first pre-fetch buffer having a first buffer fill watermark;

18 setting up a second pre-fetch buffer corresponding to the second  
19 delayed transaction, the second pre-fetch buffer having a second buffer fill  
20 watermark;

21 monitoring each of the first and second pre-fetch buffers to determine if  
22 the fill lever of a buffer meets or exceeds its buffer fill watermark, that pre-  
23 fetch buffer being a first filled buffer;

24 and in response thereto,

25 connecting the multi-channel PCI device to the secondary bus unit;  
26 mapping a virtual buffer to the first filled buffer;  
27 transferring data from the first filled buffer to the multi-channel PCI  
28 device until the first filled buffer is empty; and  
29 disconnecting the multi-channel PCI device from the secondary bus  
30 unit.

1 23. The computing platform of claim 22, wherein the host-to-PCI bridge further  
2 comprises programmed logic to perform operations including:  
3 determining that a pre-fetch buffer other than the first filled buffer has been  
4 filled to meet or exceed its buffer fill watermark, said pre-fetch buffer being a second  
5 filled buffer;  
6 and in response thereto,  
7 connecting the multi-channel PCI device to the secondary bus unit;  
8 mapping the virtual buffer to the second filled buffer;  
9 transferring data from the second filled buffer to the multi-channel PCI  
10 device until the second filled buffer is empty; and  
11 disconnecting the multi-channel PCI device from the secondary bus  
12 unit.

1 24. The computing platform of claim 22, wherein the host-to-PCI bridge further  
2 comprises a configuration register to store a buffer fill watermark value.

1 25 The computing platform of claim 22, further comprising an integrated multi-  
2 channel PCI device coupled to the PCI bus.



1 26. The computing platform of claim 25, wherein the integrated multi-channel PCI  
2 device comprises a dual channel SCSI (Small Computer System Interface)  
3 controller.

1 27. The computing platform of claim 22, wherein the host-to-PCI bridge is  
2 integrated on a platform chipset.